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11/23/98

Using the National CLC014 Cable Equalizer at 160 Mbit/s

A series of tests were run using the Muon PDT Control Board (CB) as a data source, 360 feet of ASTRO cable connecting the CB to the latest version of the Muon Readout Card (MRC) which uses a CLC014 as a cable equalizer. The previous version of the MRC used a passive peaking network. The advantage of the CLC014 is that it adapts to whatever length cable is attached to it, while the passive network must have specific values for each cable length. A communication from Nevis Labs stating that their HOTLink test setup was giving bit errors every few minutes prompted us to begin looking at the new MRC error bit rate.

The CLC014 cable equalizer has a stated maximum operating rate of 650 Mbit/s, which is far in excess of the 160 Mbit/s that we are using. I have found the inputs of this device to be very sensitive to some sort of interference which I was unable to observe with an oscilloscope either at the input pins or at the output eye monitor (OEM) pin of the device. With the input circuit recommended by the data sheet, there were bit errors every few seconds. If I disabled the 53MHz RF and encoded clock outputs which are driven out the same strip coax used for the HOTLink data, the error rate went down, but only to one every minute or so, about the same as at Nevis. The signal at the OEM pin was much cleaner with the clock signals disabled, but that evidently is not significant.

The obvious thing to try is to lower the range of frequencies that may be present at the inputs. To that end, our first test involved just raising the value of the series resistors from the recommended 100Ω to 470Ω. The error rate dropped to a lower value - something on the order of one error every few hours while running in test mode. The variable environmental noise sources present in the DAB at this time makes it difficult to get consistent results. One test may run for a day with no errors, but a second test run a day later may give several errors over the same interval.

The next test used the input arrangement shown in Fig. 1. Several 18 hour runs with the HOTLink transmitter and receivers run with their built in self test function enabled give no errors. This translates by my reckoning to about a 10^{-12} bit error rate. To do a statistically significant bit error rate measurement many channels will need to be run at once.

The CLC014 data sheet contains a list of specific recommendations, the majority of which are standard high frequency analog techniques. One recommendation is unusual however, stating that there should be no ground plane under the input or the output pins. Since the note implicitly assumes a two-layer board, one may assume that any plane (power or ground) should be kept away from these pins. It should be noted that the MRC does not if fact have its planes cut away from these pins and it functions satisfactorily with the input network shown. It is not clear that what may be a good strategy for a two-layer board applies to the multi-layer case.

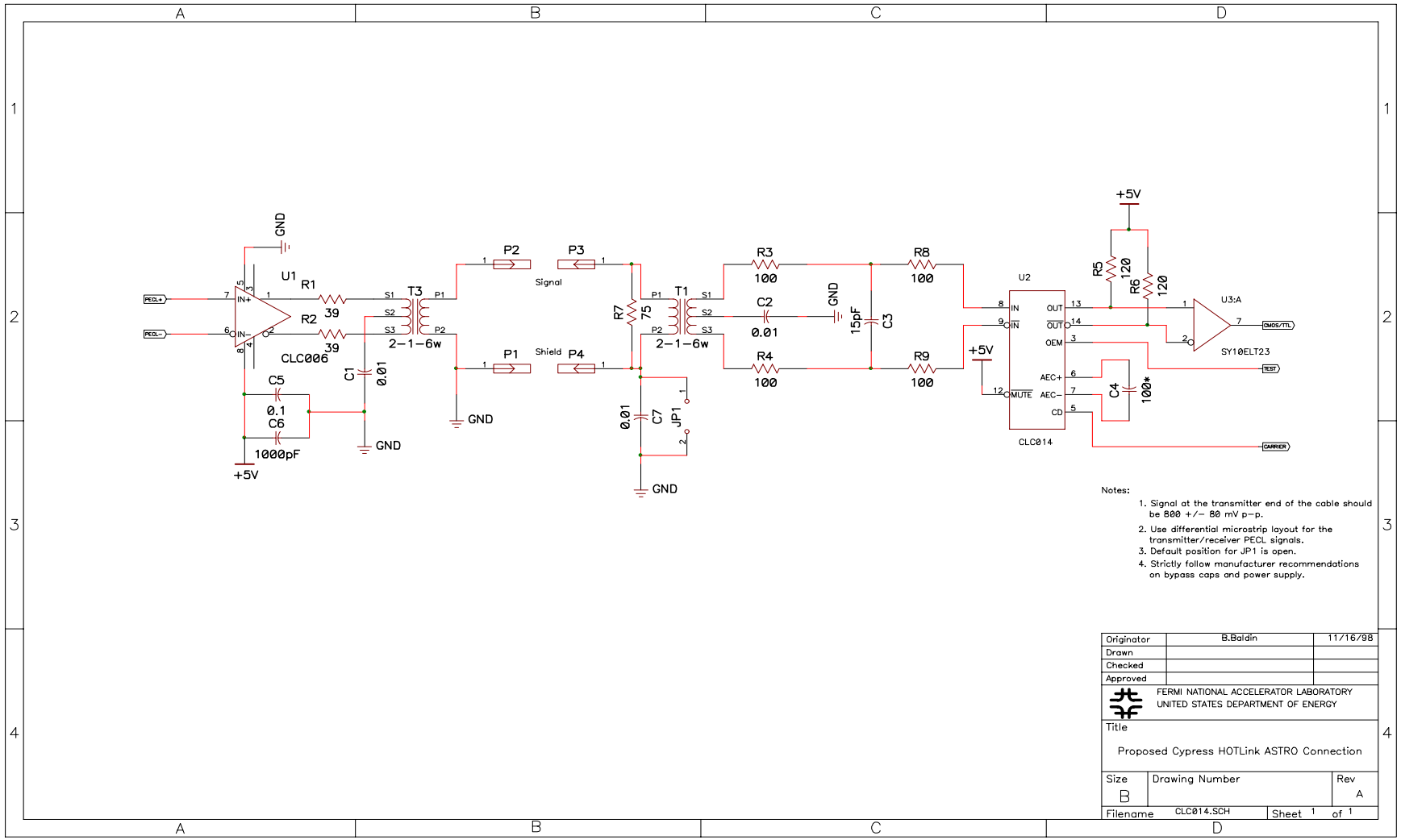

Figure 1. Proposed Cypress HOTLink Data Connection.